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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,286	GUPTA ET AL.	
	Examiner	Art Unit	
	Andrew Lai	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/11/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 8 recites "*...masking a data read request... when the counter value is at least equal to and greater than a positive value of the pre-determined output data bus width; and generating an additional data read request ... when the counter value is at least equal to and less than a negative value of a pre-determined output data bus width*".

The specification does not appear to have taught the above features. The closest description in the Specification page 29 paragraph [0056], which however discloses "if the counter value is equal to and/or greater than the positive value of the pre-determined output data bus width the request modifier circuitry 631 ... generates an additional data read request ... if the counter value is equal to and/or less than the negative value of the pre-determined output data bus width then the request modifier circuitry 631 ... masks a data read requests ..."

In other words, the Specification appears to teach jus the opposite of Claim 8, which in fact is Claim 7. Examiner is unable to find any other places throughout the

Specification that teaches Claim 8. Therefore, there won't be no further Office Action for Claim 8, which however should not be construed as indication allowable subject matter.

Claim 7 recites "... *masking ... when the counter value is at least equal to and less than a negative value of ... generating ... when the counter value is at least equal to and greater than a positive value of*".

It should be noted, as a matter of mathematically possible or not, that any real value can be **either** less/greater than **or** equal to another number but can never be both less/greater than **and** equal to the number. In view of this mathematically impossible situation as well as in light of the Specification, claim 7 is therefore interpreted as "... *masking ... when the counter value is at least equal to or less than a negative value of ... generating ... when the counter value is at least equal to or greater than a positive value of*", and subsequent Office Action will be subject to this interpretation.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

4. Claims 7 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 (after interpreting it as said above in paragraph 2) recites "... *masking ... when the counter value is at least equal to or less than a negative value of the pre-determined output data bus width; and generating ... when the counter value is at least equal to or greater than a positive value of the pre-determined output data bus width*".

Here, the word "*a*" render's the claim unclear and indistinct because "*the pre-determined output data bus width*" is a fixed threshold value, in light of the Specification. The phrase of "*a negative/positive value of the pre-determined output data bus width*" says nothing either about a definite/specific value or a range thereof. It appears, in light of the Specification, the word "*a*" should be "*the*" so that claim 7 reads: "... *masking ... when the counter value is at least equal to or less than the negative value of the pre-determined output data bus width; and generating ... when the counter value is at least equal to or greater than the positive value of the pre-determined output data bus width*". This then indicates clearly using "± pre-determined output data bus width" as the threshold value to determine if *masking* or *generating* operation should be performed.

Claim 10 appears, firstly, to have an inappropriate dependency on claim 8. The more appropriate dependency should be on claim 9. Secondly, the recitation "*substantial full is determined using a number of stages of pipeline subtracted from a capacity of the output FIFO*" provides no clear explanation how the *number of stages of pipeline* can logically be subtracted from the *capacity of the output FIFO*. The Specification appears have merely repeated the recitation here. For such subtraction to be logically meaningful, the "capacity of the output FIFO" will have to be measured in units of the "stages of pipeline". The Specification appears to be silent on this. Therefore, in light of the principle of the Specification, Examiner is compelled to interpret the claim as being "*substantial full is determined by an upper limit resulting from a subtraction from a capacity of the output FIFO*" and subsequent Office Action will based on this interpretation.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-6, 11-12, 15-16, 20 and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Minoda (US 5,731,770).

Minoda discloses "a digital data buffering device" (col. 1 lines 4-5, and see fig. 6, which depicts "a block diagram showing the schematic structure" thereof, as recited col. 3 lines 33-34) having (see fig. 6) "An input rate calculator 205 (average rate calculating means), the clock generator 206 (transfer rate controlling means), and a read address generator 204 (second address generating means)" (col. 6 lines 44-47) and further comprising the following features:

Regarding claim 1, *a method* ("correction method", col. 8 line 4), *comprising calculating a variation between an input data rate and a predetermined output data rate* (refer to fig. 6 and see "with the structure of the input rate calculator 205, the average of input rates of data after the conversion of the sampling rate in a given period of time, and the difference between the average input rate and a reference output rate are calculated", col. 7 lines 20-24), *the input data rate being based on a number of data read requests* (see "count n represents a value corresponding to the average input rate in a given period... The reference value N indicates a value corresponding to the

reference output rate.", col. 7 lines 33-34, which *n* is a result of counting the data read into the buffer as the follows, in reference to fig. 9 showing internal structure of input rate calculator 205, "the pulse signal a_1 is input to the counter 501 from the write address generator 202. The counter 501 counts the number of pulses of the pulse signal a_1, and inputs the count *n* to the latch section 502 ... the latch section 502 latches the count *n* counted just before the reset and inputs the count *n* to the comparator 504", col. 7 lines 25-32).

compensating for the variation (refer to fig. 7 and see "correcting the difference between the average input rate and the reference output rate according to the content of the correction rate table 301", col. 8 lines 14-16, and further "matches the difference between the average input rate and the reference output rate", col. 8 lines 22-23) *by modifying the number of data read requests* (see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52 and further "the clock generator 206 is provided with a correction rate table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference between the average input rate ... and the reference output rate", col. 8 lines 2-6, which then effectively *modifies the number of data read requests* because the clock generator, as disclosed, will provide the corrected clocks to read address generator 204, which in turn generates the address for reading output data per the corrected clocks).

Claim 2, *wherein the variation is compensated to increase a bandwidth in a communication channel.*

Claim 5, *wherein modifying the number of data read requests comprises generating additional data read requests.*

(see, e.g. "When the relation between the count n and the reference value N is $n < (0.98 \times N)$, the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24, noting that said "matches the difference" in this case will have to *generate additional read requests.*).

Claim 3, *wherein the variation is compensated to increase the bandwidth in a plurality of communication channels* (see fig. 6 depicting "parallel/serial converter 207" which suggests *a plurality of communication channels*).

Claim 6, *wherein modifying the number of data read requests comprises masking data read requests* (see, e.g. "When the relation between the count n and the reference value N is $n > (1.02 \times N)$, the count n is judged to be (+2%), i.e., 2% ahead of the reference value N", col. 7 lines 54-56, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24, noting that said "matches the difference" in this case will have to *mask additional read requests*).

Claim 11, *comparing a total bit group of data received* ("count n" cited above) *by a packet encapsulator* ("digital data buffering device" cited above) *from a data read request with a counter value* ("reference value N" cited above) (see fig. 9 "comparator 504" taking said "count n" and "reference value (N)" as inputs for *comparing*); *and*

performing at least one of making a data read request and generating an additional data read request (see "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]").

Claim 12, *wherein the total bit group of data is a byte* (it is notorious old and well known in the art that digital data formed with information in bits and bytes wherein each byte has eight bits).

Regarding claim 15, *an apparatus* (see "a digital data buffering device", col. 1 lines 4-5, as depicted in fig. 6), *comprising:*

an encapsulator engine (fig. 6 "read address generator 204"); *and*

a packet pre-processor (fig. 6 "input rate calculator 205", "address selection/read and write timing generator 203" and "clock generator 206") *coupled to the encapsulator engine* (fig. 6 depicting such coupling), *the packet pre-processor to calculate a variation between an input data rate and a pre-determined output data rate* (fig. 6 and see "with the structure of the input rate calculator 205, the average of input rates of data after the conversion of the sampling rate in a given period of time, and the difference between the average input rate and a reference output rate are calculated", col. 7 lines 20-24), *the input data rate being based on a number of data read requests* (see "count n represents a value corresponding to the average input rate in a given period. The reference value N indicates a value corresponding to the reference output rate.", col. 7 lines 33-34, which n is a result of counting the data read in as the follows, in reference to fig. 9 showing internal structure of input rate calculator 205, "the pulse signal a_1 is input to the counter 501 from the write address generator 202. The counter 501 counts

the number of pulses of the pulse signal a_1, and inputs the count n to the latch section 502 ... the latch section 502 latches the count n counted just before the reset and inputs the count n to the comparator 504", col. 7 lines 25-32), *the packet pre-processor to compensate for the variation* (refer to fig. 7 and see "the clock generator 206 is provided with a correction table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference between the average input rate and the reference output rate according to the content of the correction rate table 301", col. 8 lines 14-16, and further "matches the difference between the average input rate and the reference output rate", col. 8 lines 22-23) *by modifying the number of data read requests* (see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52 and further "the clock generator 206 is provided with a correction rate table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference between the average input rate ... and the reference output rate", col. 8 lines 2-6, which then effectively *modifies the number of data read requests* because the clock generator, as disclosed, will provide the corrected clocks to read address generator 204, which in turn generates the address for reading output data per the corrected clocks).

Claim 16, *a pre-compute circuitry* (fig. 7 "counter 501" and "latch section 502") *to calculate a total bit group of data received* ("count n" cited above and shown in fig. 7 as output from said "latch section 502", for which see "The latch section 502 latches the count n counted by the counter 501", col. 7 lines 5-6) *by the packet pre-processor at the*

input data rate (see "The count *n* represents a value corresponding to the average input rate in a given period", col. 7 lines 33-34); *and*

a request modifier circuitry (fig. 7, "comparator 504" and "clock generator 206") *coupled to the pre-compute circuitry* (fig. 7 depicting such coupling), *the request modifier circuitry to determine a difference between the total big group of data calculated by the pre-compute circuitry* (fig. 7 depicting "count *n*" as an input to said "comparator 504") *and a predetermined output data bus width* (fig. 7 "reference value (*N*)", and see further "The comparator 504 compares the count *n* latched by the latch section 502 and the reference value '*N*' to determine the difference therebetween, and output the result to the clock generator 206 in a later stage", col. 7 lines 16-19).

Regarding claim 20, *an apparatus* (see "a digital data buffering device", col. 1 lines 4-5, and fig. 6, which depicting such), *comprising:*

means for transmitting data through a communication channel (fig. 6 "parallel/serial converter 207", which "outputs data ... to be input to a D/A converter", col. 6 lines 29-31) *having a bandwidth* (see "The reference value *N* indicates a value of corresponding to the reference output rate", col. 7 lines 35-36, noting that an output rate "*N*" necessarily indicates/requires matching *bandwidth*);

means for modifying data read requests (fig. 6 "clock generator 206", which, referring to fig. 7, is responsible "for correcting the difference between the average input rate ... and the reference output rate [the '*N*' value hereinabove]", col. 8 lines 4-6, noting that as shown in fig. 6 the "clock generator 206" controls "read address generator 204", which is "for generating the address of output data according to clocks generated by the

clock generator 206", col. 6 lines 50-52, and it is well known in the art that "read addresses" is generated per read requests, noting also that "[a] count n represents a value of corresponding to the average input rate", col. 7 lines 33-34) *transmitted by a framer engine* (fig. 6 "input rate calculator 205" wherein "the average of input rates of data after the conversion of the sampling rate in a given period of time ... are calculated", col. 7 lines 20-24, and, as shown in fig. 6, *transmitted* to the "clock generator 206"); *and*

means for increasing a utilization efficiency of the bandwidth (see, e.g., "When the relation between the count n and the reference value N is $n < (0.98 \times N)$, the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24, which is effectively *increasing utilization efficiency of the bandwidth*).

Regarding claim 23, *a system* (fig. 1, "a sampling rate converter", col. 3 line 17), *comprising:*

a link layer device (fig. 1 the portion between "input interface 2" and "output interface 8", which portion, "link portion" hereinafter, links the "input interface 2" and the "output interface 8" as shown in fig. 1);

a first physical interface device (fig. 1 "input interface 2"); *and*

a framer (fig. 6, a "digital data buffering device", col. 3 line 34, which "is applied to the output interface 8 [of fig. 1]", col. 6 line 24) *coupled to the link layer device* (said "link portion" of fig. 1) *and the first physical interface device* (said "input interface 2" of fig. 1),

wherein the framer comprises an encapsulator engine (fig. 6 "parallel/serial converter 207") *and a packet pre-processor* (fig. 6 items 201-206, "pre-processor" hereinafter, comprising, e.g., "write address generator 202", "input rate calculator 205, "clock generator 206", "read address generator 204", etc.) *coupled to the encapsulator engine* (fig. 6 depicting the coupling between the "pre-processor" and "parallel/serial converter 207"), *the packet pre-processor to calculate a variation between an input data rate and a pre-determined output data rate* (see "with the structure of the input rate calculator 205, the average of input rates of data after the conversion of the sampling rate in a given period of time, and the difference between the average input rate and a reference output rate are calculated", col. 7 lines 20-24), *the input data rate being based on a number of data read requests* (see "count n represents a value corresponding to the average input rate in a given period... The reference value N indicates a value corresponding to the reference output rate.", col. 7 lines 33-34, which n is a result of counting the data read into the buffer as the follows, in reference to fig. 9 showing internal structure of input rate calculator 205, "the pulse signal a_1 is input to the counter 501 from the write address generator 202. The counter 501 counts the number of pulses of the pulse signal a_1, and inputs the count n to the latch section 502 ... the latch section 502 latches the count n counted just before the reset and inputs the count n to the comparator 504", col. 7 lines 25-32), *the packet pre-processor to compensate for the variation* (refer to fig. 7 and see "the clock generator 206 is provided with a correction rate table 301. The correction rate table 301 stores a correction method as a table, for correcting the difference between the average input rate and the reference

output rate according to the content of the correction rate table 301", col. 8 lines 14-16, and further "The speed correction amount calculator 303 matches the difference between the average input rate and the reference output rate", col. 8 lines 22-23) *by modifying the number of data read requests* (see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52, which then effectively *modifies the number of data read requests* because the clock generator, as disclosed, will provide the corrected clocks to read address generator 204, which in turn generates the address for reading output data per the corrected clocks).

Claim 24, *the packet pre-processor* ("pre-processor" of fig. 6 as discussed above for claim 23) *comprises:*

a pre-compute circuitry (fig. 7 "counter 501" and "latch section 502") *to calculate a total bit group of data received* ("count *n*" cited above and shown in fig. 7 as output from said "latch section 502", for which see "The latch section 502 latches the count n counted by the counter 501", col. 7 lines 5-6) *by the packet pre-processor at the input data rate* (see "The count *n* represents a value corresponding to the average input rate in a given period", col. 7 lines 33-34); *and*

a request modifier circuitry (fig. 7 "comparator 504" and "clock generator 206") *coupled to the pre-compute circuitry* (fig. 7 depicting such coupling), *the request modifier circuitry to determine a difference between the total big group of data calculated by the pre-compute circuitry* (fig. 7 depicting "count *n*" as an input to said "comparator 504") *and a predetermined output data bus width* (fig. 7 "reference value

(N)", and see further "The comparator 504 compares the count n latched by the latch section 502 and the reference value 'N' to determine the difference therebetween, and output the result to the clock generator 206 in a later stage", col. 7 lines 16-19).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda (US 5,731,770) in view of Norizuki et at (US 5,357,510, Norizuki hereinafter)

Minoda discloses claimed limitations as discussed above in paragraph 6 for claims 1 and 20 respectively including *the variation is compensated.* Minoda does not disclose the following features:

for claim 4, [the variation is compensated] *to decrease a number of idle cell insertions;*

for claim 21, *means for decreasing a number of idle cell insertions.*

Norizuki discloses "an apparatus for supervising and controlling ATM traffic" (Abstract lines 1-2) having a "control unit for performing the operation of traffic control in accordance with the idle cell rate provided" (Abstract lines 15-16) comprising for

Claim 4, [the variation is compensated] *to decrease a number of idle cell insertions;*

Claim 21, *means for decreasing a number of idle cell insertions.*

(refer to figs. 6 and 7 and see "fig. 7 shows an example of a variation of the ratio of idle cells to user information cells on a transmission line ... and a total band width consists of an idle cell band width and a user band width", col. 6 lines 31-36, noting that fig. 7 shows in some cases idle cells are inserted *to a decreased number* than some other cases).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method/apparatus of Minoda by adding the idle cell insertion feature of Norizuki to Minoda in order to provide more instantaneously responsive system "for traffic supervisory control that ordinarily monitors the band capacity of a transmission line ... to also be able to cope with burst conditions of the traffic fluctuation" (Norizuli, col. 3 lines 41-47).

9. Claims 9, 13, 14 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda (US 5,731,770) in view of Modelski et at (US 2002/0120798, Modelski hereinafter)

Minoda discloses claimed limitations discussed above in paragraph 6 for claim 1. Minoda further discloses for

Claim 9, *transmitting an output data stream to an output* buffer (fig. 6 "ring buffer memory 201");

passing the data read requests to an input buffer (fig. 6 "ring buffer memory 201", and see "The read address generator 204 is a circuit for generating the address of

output data according to clocks generated by the clock generator 206", col. 6 lines 50-52, which effectively *passes read requests* as well known in the art) *when the output* buffer *is not substantially full* (this is well known in the art as well as intuitive also).

Claim 13, *passing the data read request to an input* buffer (fig. 6 "ring buffer memory 201", and see "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52, which effectively *passes read requests* as well known in the art).

Claim 14, *passing the data read request and the additional data read request to an input* buffer (fig. 6 "ring buffer memory 201", and see, for *the data read request*, "The read address generator 204 is a circuit for generating the address of output data according to clocks generated by the clock generator 206", col. 6 lines 50-52, which effectively *passes read requests* as well known in the art; and see further, for *the additional data read request* , e.g., "When the relation between the count n and the reference value N is $n < (0.98 \times N)$, the count n is judged to be (-2%), i.e., 2% behind the reference value N", col. 7 lines 41-43, and then "The speed correction amount calculator 303 matches the difference between the average input rate [n] and the reference output rate [N]", col. 8 lines 22-24, which inevitably results in *additional read request*).

Claim 17, *a link layer device* (fig. 6 "write address generator 202");

an input buffer (fig. 6 "ring buffer memory 201") *coupled to the request modifier circuitry* (fig. 7, "comparator 504" and "clock generator 206"), *link layer device* (fig. 6 "write address generator 202") *and the pre-compute circuitry* (fig. 7 "counter 501" and "latch section 502", and fig. 6 depicting such coupling), *the input* buffer *to receive input*

data at the input data rate (fig. 6 depicting "ring buffer memory 201" receiving "data after sampling rate conversion"); *and*

an output buffer (fig. 6 "ring buffer memory 201") *coupled to the encapsulator engine and the request modifier circuitry* (fig. 6 depicting said coupling), *the output* buffer *to transmit output data* (fig. 6 "DA data") *at the predetermined output data rate* (see "correcting the difference between the average input rate and the reference output rate", col. 8 lines 14-15).

Claim 18, *a frame engine* (fig. 6 "parallel/serial converter 207") *coupled to the output* buffer (fig. 6 "ring buffer memory"); *and*

a physical interface (fig. 1 "output interface 8") *device coupled to the frame engine* (noting that said "parallel/serial converter" as part of the "digital data buffering device" shown in fig. 6 "is applied to the output interface 8 [of fig. 1]", col. 6 line 24)

Claim 19, *the pre-compute circuitry receives input data from the input* buffer, *the encapsulator engine receives the input data from the pre-compute circuitry, the output* buffer *receives the output data from the encapsulator engine, the request modifier circuitry receives data read requests from the frame engine, the link layer device receives the data read request from the request modifier circuitry* (figs. 6, 7 and 9 in combination depicting such data flow steps, noting the fact that Minoda's "ring buffer memory" plays a dual role of input/output buffers).

Minoda does not disclose:

for claims 9, 13, 14, 17-19, said intput/output buffers are of *first-in-first-out (FIFO);*

for claim 9, *determining when the output FIFO is substantially full;*

masking the data read request to the input FIFO when the output FIFO is substantially full.

Modelski discloses a "Global access bus architecture includes a master request bus and a slave request bus separated from each other and pipelined" (Abstract lines 1-2) wherein "pipelines operate on the read request" ([0203] lines 5) comprising the above cited features missing from Minoda, particularly for:

Claims 9, 13, 14, 17-19, using separate intput/output *FIFOs* (see "input and output FIFOs buffer");

Claim 9, *determining when the output FIFO is substantially full; and masking the data read request to the input FIFO when the output FIFO is substantially full* (see "The input and output FIFOs buffer data flow between the pipelines and the MUXs. Since lookups and filters can be forwarded from one [memory] bank to the other (depending on the contents of the back forwarding registers), a lockout condition can occur where the output FIFOs for each bank are full and each input FIFO has a lookup that needs to continue ... This is controlled by the MUXs that do not allow more than 32 operations to be submitted across both pipelines", [0204] lines 1-9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Minoda by adding Modelski's input/output FIFO and lookup lockout mechanism upon detecting a full output FIFO being in order to provide a more robust method/device which further "provides fast path processing and enhanced flexibility/adaptability of packet processors" (Modelski, [0013] lines 4-5).

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda (US 5,731,770) in view of Modelski et at (US 2002/0120798, Modelski hereinafter), as applied above to claim 9, and further in view of Rajaraman (US 5,802,310).

Minoda in view of Modelski discloses claimed limitations discussed above in paragraph 9 including Modelski disclosing using output FIFO and determining the fullness of the FIFO. Minoda in view of Modelski however does not disclose *substantial full is determined by an upper limit resulting from a subtraction from a capacity of the output FIFO.*

Rajaraman discloses "systems and methods for data channel queue control in a communications network" (col. 1 lines 1-3) wherein, refer to fig. 5, "data transfer controlling 54" to "queue 56" is based on "queue limit determining 58". Rajaraman's methods further comprises *substantial full is determined by an upper limit resulting from a subtraction from a capacity of the output FIFO* (see firstly, "more commonly, a 'high-water mark" (HWM) less than the queue capacity and a 'low-water mark' (LWM) greater than empty are established for the data store", col. 3 lines 30-33, and secondly, Rajaraman provides further improvements, see fig. 6, step 71 "is amount of queued data greater than first limit [corresponding to HWM]?" and, if the answer is "Yes", step 71a "disable data transfer from application to queue").

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method of Minoda by adding the queue limit mechanism of Rajaraman in order to provide a more efficient system "which dynamically optimize

queue parameters such as high water mark (HWM) and low water mark (LWM) in response to network and node conditions" (Rajaraman, col. 4 lines 6-8).

11. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda (US 5,731,770) in view of Kuo et at (US 6,047,001, Kuo hereinafter)

Minoda discloses claimed limitation in paragraph 6 above, particularly those applied to claim 20. Minoda does not disclose **regarding claim 22** the feature of *compensating for invalid bytes of an input data stream.*

Kuo discloses "a network interface device having a random access memory for buffering data" (Abstract lines 1-2) using a "frame information generation" unit (fig. 4 item 82) comprising *compensating for invalid bytes of an input data stream* (see, in reference to figs. 4 and 5, "the frame information generation logic 82 determines the count value (CNT) by subtracting the value of the write pointer 90, minus the address value in the start address 92, minus the invalid byte count determined from the byte enable value (BE-L) in step 106a", col. 10 line 67 – col. 11 line 5).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Minoda by adding the invalid data subtraction mechanism of Kuo to Midona in order to provide a more efficient system "enabling a read controller to quickly determine the status of a stored data frame by accessing the corresponding tracking information" (Kuo col. 3 lines 9-11).

12. Claim 25 rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda (US 5,731,770) in view of Zelikovitz et at (US 5,555,478, Zelikovitz hereinafter)

Minoda discloses claimed limitations in paragraph 6 above, particularly those applied to claim 24. Minoda further discloses for:

Claim 25, *a second physical interface device* (fig. 1 "output interface 8") *coupled to the link layer device* (said "link portion" discussed for claim 23 above), *wherein the second physical interface device, the link layer device, the framer* (fig. 6 "digital data buffering device") *and the first physical interface device* (fig. 1 "input interface") *reside in a* data processor (fig. 1 "a sampling rate converter" showing all said elements).

Minoda does not expressly disclose that said data processor ("sampling rate converter") is *a line card.*

Zelikovitz discloses a "fiber optic information transmission system" (col. 2 lines 1-2) having a "thirty two (32) subscribers linked to four (4) fiber optic cables in the fiber optic network" (fig. 2A and col. 2 lines 1-3) comprising the above feature, i.e., using *line card* as a data processor (refer to fig. 2A item 120 and see "This line card 120 is a data processor capable of manipulating data appropriately to form the transmission packet", col. 9 lines 24-25).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the device of Minoda by adding the line card feature of Zelikovitz to Minoda in order to provide a scalable system that "establishes a digital information network having a very high capacity" (Zelikovitz, col. 1 lines 57-58)

13. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Minoda (US 5,731,770) in view of Zelikovitz et at (US 5,555,478, Zelikovitz

hereinafter), as applied above to claim 25, and further in view of Duplessis et at (US 2002/0,191,617, Duplessis hereinafter)

Minoda in view of Zelikovitz discloses claimed limitations in paragraph 11 above. Minoda in view of Zelikovitz does not disclose the following features:

for claim 26, *wherein the second physical interface device is an Ethernet device and the first physical interface device is a Synchronous Optical Network (SONET) device;*

for claim 27, *wherein the line card is coupled to a wide area network (WAN).*

Duplessis discloses a "system and method for transporting channelized Ethernet over SONET/SDH" (page 1 left col. lines 1-2) using, referring to fig. 3, "a preferred network element 12 that is capable of allowing communication path between network systems Net1 and Net2" ([0020] lines 1-3, which Net1 and Net2 are shown in fig. 2) comprising the above cited features, particularly for:

Claim 26, *wherein the second physical interface device is an Ethernet device and the first physical interface device is a Synchronous Optical Network (SONET) device* (refer to figs. 3 and 4 and see "the mapper module 14 in the preferred network element 12 maps a traffic port such as an Ethernet port onto the STS-48c", [0021] lines 8-10, which "STS-48c" is a well-known SONET data standard, which is also depicted in fig. 3 by "SONET/SDH" output from "line card 18").

Claim 27, *wherein the line card is coupled to a wide area network (WAN)* (refer to fig. 2 and see "the network systems Net1, Net2, Net3, and Net4 could be local area

networks (LANs), metro area networks (MANs), wide area networks (WANs)", [0019] last four lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the method/device of Minoda by adding the SONET/Ethernet/WAN feature of Duplessis to Minoda in order to provide a more flexible and efficient method/system that is able "to map a payload size of y into x when y<<x" (Duplessis, [0005] lines 7-8).

Allowable Subject Matter

14. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 provides detailed steps of controlling *data read request* of which the following features/steps appear to be allowable subject matter:

subtracting the difference from a count value.

masking a data read quest transmitted from a packet encapsulator to the input FIFO when the counter value is at least equal to or less than the negative value of the pre-determined output data bus width; and

generating an additional data read request to be transmitted from the packet encapsulator to the input FIFO when the counter value is at least equal to or greater than the positive value of the pre-determined output data bus width (examiner's note: this would mean mathematically $D_{in} \leq C$).

It is noted that the closest prior art of Minoda and Modelski, singularly or in combination fails to anticipate above underlined features or render them obvious.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 5,761,417 discloses a video data streamer having scheduler for scheduling read request for individual data buffers associated with output ports.

US 6,286,074 provides method and system for reading prefetched data across a bridge system.

US 5,327,570 teaches a multiprocessor system having local write cache within each data processor node wherein read request is modified per node bandwidth

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Lai whose telephone number is 571-272-9741. The examiner can normally be reached on M-F 7:30-5:00 EST, Off alternative Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kwang Yao can be reached on 571-272-3182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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AL

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